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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/475,614
Filing Date: December 30, 1999
Appellant(s): WOLRICH ET AL.

Denis G. Maloney
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed January 28 2008 appealing from the Office action mailed January 19 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

The appeal on U.S. patent application 09/626,535 was withdrawn in favor of a RCE. An amendment for that application was filed on 1/29/2008 in response to a non-final rejection mailed on 11/13/2007.

(3) Status of Claims

The statement of the status of claims contained in the brief is incorrect. A correct statement of the status of the claims is as follows:

The pending claims are 1-44 (claims 26-43 have not been cancelled).

This appeal involves Group I claims 1-25 (not 1-24 as indicated in the brief) and 44.

Claims 26-43 are withdrawn from consideration (not cancelled as indicated in the brief) as not directed to the elected Group I.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is defective.

For the convenience of the Board, claim 17 is reproduced with Appellants' annotation in the summary of the invention as follow.

Annotated Claim 17

A method of receiving data from a plurality of peripheral ports (page 11, lines 11-13), comprising:

determining that the one of the plurality of peripheral ports requires servicing (page 24, lines 11-13);

issuing a receive request based on the determination (page 20, lines 12-15), the receive request directing the transfer of data from the one of the plurality of peripheral ports to a buffer memory and specifying a program thread from among of a plurality of processing program threads to process the data (page 10, line 5 to page 11 line 2); and

transferring the data to the buffer memory and signaling to the specified thread that the data is ready for processing (page 14, lines 2-4) (page 25, lines 16-22).

The summary of the invention is defective because page 11, lines 11-13 does not disclose a method of receiving data from a plurality ports having step for determining, step for issuing request and step transferring as recited in the preambles of the claims.

Pages which are identified by Appellants for the support of the steps do not disclose that they are steps of a method of receiving data from a plurality of peripheral ports. In fact, the alleged steps are disclosed in different pages of different order.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,373,848	Allison	4-2002
6,604,125	Belkin	8-2003

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-25 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Allison (USP 6,373,848) in view of Belkin (USP 6,604,125).

Appellants' Invention

Appellants' invention is a single step method. The method is to issue a request to transfer data from one of a plurality of ports to a buffer memory and to specify a thread from a plurality of threads to process the data.

Teaching of Allison

Attention of the Board is respectfully directed to the abstract, the summary of the invention in columns 2-3, Figures 1 and 9 and the description thereof and columns 4-9 in Allison. Allison teaches a multi-port adapter having a single Media Access Control (MAC) serving all ports (lines 31-33 of column 2). Figure 1 shows that the single MAC comprises a plurality of ports 0-N (column 3, line 53), a pair of FIFO registers 40 and 43 for receiving data from a plurality of ports, and a multiplexer for selecting one port from a plurality of ports. Figure 9 depicts a flow chart for showing operation of data transfer between selected one of the ports and the host via the MAC. Allison in columns 4-9 further teaches that TxMII (line 53, column 4) and RxMII (line 45, column 6) select one of a plurality of threads to process the received data dependent on whether the state machine is in IDLE state, DATA state, WAIT state, JAM state or JAM Wait state.

Rejection of the claims

Appellants provide separate arguments for independent claims 1, 17 and 18 but not dependent claims 2-16, 19-24 and 44. Dependent claims 2-16 and 44 therefore stand or fall with their parent independent claim 1 and dependent claims 19-25 stand or fall with their parent independent claim 18. Independent claim 17 has no dependent claims.

Independent claims 1 and 18 are one step method claims. Independent claim 17 is most comprehensive among claims 1, 17 and 18 and includes all the limitations of claims 1 and 18. Claim 17 therefore is selected as an exemplary in the art rejection.

Claim 17

With respect to claim 17, reference is made to the abstract, Figures 1 and 9 and the description thereof and columns 4-9 in Allison. Allison teaches:

a method (column 2, lines 43-45) of receiving data from a plurality of peripheral ports (port 0 to port N, Figure 1), comprising:

determining that the one of the plurality of peripheral ports requires servicing (see port selector 46 in Figure 1; see also Figure 9 step 100, one of the ports is selected by the selector 46 for servicing because it is determined that one of the ports requires servicing);

issuing a receive request based on the determination (based on the determination control signals are generated in Allison to control the selector 46 and the multiplexer 18 to do the following), the receive request directing the transfer of data from the one of the plurality of peripheral ports to a buffer memory (Figure 1 in Allison shows that port selector 46 together with multiplexer 18 select one port from a plurality of N ports for transferring data from the selected port to FIFO buffer memory, see column 2, last line to column 3, line 2; see step 106 of Figure 9 and the description thereof in lines 28-30 of column 11) and specifying a program thread from among of a plurality of processing program threads to process the data (see line 6 of column 4 to line 5 of column 10; Allison teaches that his system has several states such as IDLE State,

PREAMBLE State. DATA State, WAIT State, JAM State, and JAM Wait State, etc and dependent on the state, one of the groups of control instructions each associated with a specific state is selected to control the system. For example, if the system is currently in DATA State, the group of instructions associated with DATA State is selected to control the system to operate in a manner as set forth in lines 33-45 of column 5. If the system is in other states, other groups of instructions are selected, etc.) and

transferring the data to the buffer memory (transferring data from the selected one of N ports to RxFIFO or TXFIFO) and signaling to the specified thread that the data is ready for processing.

Obviousness: Allison does not appear to organize the plurality of groups of instructions into a multithread environment.

The only difference is that it is not clear whether the plurality of groups of instructions in Allison is organized in a multithread environment. Belkin teaches in lines 18 et seq. of column 1 that:

> "Many of today's high capacity computers, such as web servers, are required to process a large number of requests concurrently. To enable them to do so efficiently, many of these computer systems implement a technique known as multi-threading"

Since Allison has a large number of states and therefore requests, it would have been obvious to a person of ordinary skill in the art to have the system of Allison to be organized in a multithread environment so that the system is run more efficiently.

Claims 2-16 and 44

Claims 2-16 and 44 stand or fall with independent claim 1.

Claims 19-25

Claims 19-25 stand or fall with independent claim 18.

(10) Response to Argument

Appellants' remarks from page 7 to line 3 of page 10 are considered moot because they are not arguments. Those pages contain citations of the authorities and what they understand of Allison's disclosure.

Claims 1 and 18

Appellants contend that Allison does not teach:

> issuing a receive request based on the determination,
> the receive request directing the transfer of data from
> the one of the plurality of peripheral ports to a buffer memory"

The Examiner disagrees. The request is not actually a request. The request as recited is actually a command instructing the system to transfer data from one of a plurality of ports to a buffer memory. It is a command because there are no steps recited for accepting or rejecting the request and no steps for deciding what to do if the request is accepted or rejected. The claims recite that data is transferred in response to the request. The request therefore is a command. Reference is now made to Allison. In Figure 9 of Allison, data is transferred from one of a plurality of ports to a buffer memory. The command in Allison is generated when it is determined that one of a plurality of ports requires service because the port has data waiting to be transferred. Allison therefore meets the claim limitation.

Appellants contend that Allison does not teach:

> specifying a program thread from among of a plurality of processing program threads to process the data

The Examiner disagrees. Reference is made to the 103 Rejection above. Allison teaches a plurality of groups of instructions for processing the data depending on the state of the machine. If the groups of instructions are organized in a multithread environment as taught by Belkin, a thread would be selected from among a plurality of threads for processing the data so that the system would run more efficiently.

Claim 17

The second step of claim 17 is the same single step recited in claims 1 and 18. Appellants do not provide any argument as to why the rest of the steps other the second step are patentable over the applied references. It appears that Appellants rely on the second step of claim 17 for patentability. Claim 17 therefore stands or falls with claims 1 and 18.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

(12) Conclusion

As set forth in the summary of the invention above, pages which are identified by Appellants for the support of the steps do not disclose that they are steps of a method of receiving data from a plurality of peripheral ports. In fact, the alleged steps are disclosed in different pages of different order.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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